UNITED STATES PATENT APPLICATION

OF

Bin YU

and

Shibly S. AHMED

FOR

METHOD FOR FORMING A TRI-GATE MOSFET

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FIELD OF THE INVENTION

[0001] The present invention relates generally to semiconductor manufacturing and, more particularly, to forming metal oxide semiconductor field effect transistor (MOSFET) devices.

BACKGROUND OF THE INVENTION

[0002] The escalating demands for high density and performance associated with ultra large scale integration semiconductor devices require design features, such as gate lengths, below 100 nanometers (nm), high reliability and increased manufacturing throughput. The reduction of design features below 100 nm challenges the limitations of conventional methodology.

[0003] For example, when the gate length of conventional planar MOSFETs is scaled below 100 nm, problems associated with short channel effects, such as excessive leakage between the source and drain, become increasingly difficult to overcome. In addition, mobility degradation and a number of process issues also make it difficult to scale conventional MOSFETs to include increasingly smaller device features. New device structures are therefore being explored to improve FET performance and allow further device scaling.

[0004] Double-gate MOSFETs represent new structures that have been considered as candidates for succeeding existing planar MOSFETs. In double-gate MOSFETs, two gates may be used to control short channel effects. A FinFET is a double-gate structure that exhibits good short channel behavior. A FinFET includes a channel formed in a vertical fin. The FinFET structure may also be fabricated using layout and process techniques similar to those used for conventional planar MOSFETs.

SUMMARY OF THE INVENTION

[0005] Implementations consistent with the principles of the invention provide a tri-gate MOSFET device that provides better short-channel control than double and single gate device designs.

[0006] In accordance with the purpose of this invention as embodied and broadly described herein, a method for forming a tri-gate semiconductor device that includes a substrate and a dielectric layer formed on the substrate includes depositing a first dielectric layer on the dielectric layer and etching the first dielectric layer to form a structure. The method further includes depositing a second dielectric layer over the structure, depositing an amorphous silicon layer over the second dielectric layer, etching the amorphous silicon layer to form amorphous silicon spacers, where the amorphous silicon spacers are disposed on opposite sides of the structure, depositing a metal layer on at least an upper surface of each of the amorphous silicon spacers, annealing the metal layer to convert the amorphous silicon spacers to crystalline silicon fin structures, removing a portion of the second dielectric layer, depositing a gate material, and etching the gate material to form three gates.

[0007] In another implementation consistent with the present invention, a method of manufacturing a semiconductor device that includes a substrate and a nitride layer formed on the substrate is disclosed. The method includes depositing a first silicon oxide layer on the nitride layer; etching the first silicon oxide layer to form a structure, where the structure includes at least a first side surface, a second side surface, and a top surface; depositing a second silicon oxide layer over the top surface and surrounding the first and second side surfaces of the structure; depositing an amorphous silicon layer over the second silicon oxide layer; etching the amorphous silicon layer to form amorphous silicon structures, where a first amorphous silicon structure is formed on a first side of the structure and a second amorphous silicon structure is formed on a second side of the structure; depositing a metal layer on at least an upper surface of

each of the amorphous silicon structures; performing a metal-induced crystallization operation to convert the amorphous silicon structures to crystalline silicon structures; removing a portion of the second silicon oxide layer; forming a source region and a drain region; depositing a gate material over at least the crystalline silicon structures; and patterning and etching the gate material to form three gate electrodes.

[0008] In yet another implementation consistent with the principles of the invention, a semiconductor device is disclosed. The semiconductor device includes a structure comprising a dielectric material and including a first side and a second side; a first fin structure comprising a crystalline silicon material and being formed adjacent to the first side of the structure; a second fin structure comprising the crystalline silicon material and being formed adjacent to the second side of the structure; a source region formed at one end of the structure, the first fin structure, and the second fin structure; a drain region formed at an opposite end of the structure, the first fin structure, and the second fin structure; a first gate formed adjacent the first fin structure; a second gate formed adjacent the second fin structure; and a third gate formed above the first fin structure and the second fin structure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate an embodiment of the invention and, together with the description, explain the invention. In the drawings,

[0010] Fig. 1 illustrates an exemplary process for forming a tri-gate MOSFET device in an implementation consistent with the principles of the invention;

[0011] Figs. 2-10 illustrate exemplary views of a MOSFET device fabricated according to the processing described in Fig. 1;

[0012] Figs. 11-14 illustrate exemplary views for improving gate patterning in an alternative implementation consistent with the principles of the invention; and

[0013] Figs. 15 and 16 illustrate exemplary views for performing gate filling according to an alternative implementation consistent with the principles of the invention.

DETAILED DESCRIPTION

[0014] The following detailed description of implementations consistent with the present invention refers to the accompanying drawings. The same reference numbers in different drawings may identify the same or similar elements. Also, the following detailed description does not limit the invention. Instead, the scope of the invention is defined by the appended claims and their equivalents.

[0015] Implementations consistent with the principles of the invention provide a tri-gate MOSFET device that provides better short-channel control than double and single gate device designs.

EXEMPLARY PROCESSING

[0016] Fig. 1 illustrates an exemplary process for forming a MOSFET device in an implementation consistent with the principles of the invention. Figs. 2-10 illustrate exemplary views of a MOSFET device fabricated according to the processing described in Fig. 1. The fabrication of one MOSFET device will be described hereinafter. It will be appreciated, however, that the techniques described herein are equally applicable to forming more than one MOSFET device.

[0017] With reference to Figs. 1 and 2, processing may begin with a semiconductor device that includes a substrate 200 and a nitride layer 210 formed on substrate 200. In one implementation, substrate 200 may comprise silicon or other semiconducting materials, such as germanium, or combinations of semiconducting materials, such as silicon-germanium. Nitride layer 210 may be formed on substrate 200 to a thickness ranging from about 300 Å to about 1000 Å. In alternative implementations, layer 210 may include other dielectric materials.

[0018] A dielectric layer 220, such as a silicon oxide layer, may be formed over nitride layer 210 (act 105). In one implementation, dielectric layer 220 may comprise SiO_2 and may be deposited using chemical vapor deposition (CVD) to a thickness ranging from about 600 Å to about 1000 Å. In other implementations consistent with the present invention, layer 220 may consist of other films or materials that may be deposited or grown, including conductive materials or other non-conductive materials.

[0019] SiO_2 layer 220 may be patterned and etched to form SiO_2 structure 310, as illustrated in Fig. 3 (act 110). For example, to form SiO_2 structure 310, a mask may be formed over a portion of dielectric layer 220 and dielectric layer 220 may then be etched in a conventional manner, with the etching terminating on nitride layer 210 to form SiO_2 structure 310. The resulting SiO_2 structure 310 may have a width ranging from about 500 Å to about 2000 Å.

[0020] A second dielectric layer 410 may then be formed on the semiconductor device, as illustrated in Fig. 4 (act 115). In one implementation, second dielectric layer 410 may comprise SiO_2 and may be deposited using CVD to a thickness ranging from about 200 Å to about 300 Å. In other implementations consistent with the present invention, layer 410 may consist of other films or materials that may be deposited or grown, including conductive materials or other non-conductive materials.

[0021] An amorphous silicon layer 510 may be formed over second SiO_2 layer 410, as illustrated in Fig. 5 (act 120). In one implementation, amorphous silicon layer 510 may be deposited to a thickness ranging from about 150 Å to about 300 Å. Amorphous silicon layer 510 may then be patterned and etched to form spacers 610, as illustrated in Fig. 6 (act 125). As illustrated, spacers 610 are formed on opposite sides of SiO_2 structure 310. The width of each spacer 610 may range from about 50 Å to about 200 Å.

[0022] A metal layer 710, such as nickel, may be deposited on the semiconductor device, as illustrated in Fig. 7 (act 130). In one implementation, nickel layer 710 may be deposited to a thickness of about 20 Å to about 30 Å.

[0023] A metal-induced crystallization (MIC) operation may be performed. The MIC operation may include annealing nickel layer 710 at about 500 °C to about 550 °C for several hours, which acts to diffuse the nickel into the amorphous silicon of spacers 610 and to convert the amorphous silicon in spacers 610 to single-crystal or polycrystalline silicon fin structures 810, as illustrated in Fig. 8 (act 135). In one implementation, the annealing occurs for about 1 to 5 hours. Undiffused portions of nickel layer 710 may be removed from the semiconductor device (act 140). The undiffused portions may be removed via etching or other well-known techniques.

[0024] Portions of second SiO_2 layer 410 may then be removed, resulting in the configuration illustrated in Fig. 8 (act 145). In one implementation, the portions of second SiO_2 layer 410 located below fin structures 810 and on nitride layer 210 may be removed using a wet etch chemistry. The particular etchant(s) associated with etching second SiO_2 layer 410 may be optimized based on the particular end device requirements. Once removed, a gap exits between fin structures 810 and nitride layer 210. In one implementation, the gap may range from about 100 Å to about 500 Å.

[0025] A gate dielectric layer (not shown) may optionally be deposited or thermally grown on crystalline silicon fin structures 810. The gate dielectric layer may be formed at a thickness ranging from approximately 5 Å to 30 Å. The gate dielectric layer may include conventional dielectric materials, such as an oxide (e.g., silicon dioxide). In other implementations, a nitride material, such as a silicon nitride, may be used as the gate dielectric material.

[0026] A gate material layer 910 may then be deposited and etched to form one or more gate electrodes, as illustrated in Fig. 9 (act 150). In an exemplary implementation, gate material layer 910 may include polysilicon deposited using conventional CVD to a thickness ranging from about 200 Å to about 1000 Å. Alternatively, other semiconducting materials, such as germanium or combinations of silicon and germanium, or various metals may be used as the gate material. In one implementation, gate material layer 910 is patterned and etched to form three gate electrodes. First and second gate electrodes may be located on opposite sides adjacent the respective fin structures 810 and a third gate electrode may be located above fin structures 810.

[0027] Source/drain regions may be formed at the respective ends of fins 810. It should be understood that in some implementations, source/drain regions may be formed at an earlier processing step. Fig. 10 illustrates an exemplary top view of the semiconductor device consistent with the principles of the invention after the source/drain regions and gate electrodes are formed. As illustrated, the semiconductor device includes a triple-gate structure with fins 810, source and drain regions 1010 and 1020, and gate electrodes 1030, 1040, and 1050. Any one of gate electrodes 1030, 1040, and 1050 may be used to bias the semiconductor device during circuit operations.

[0028] Source/drain regions 1010 and 1020 may then be doped with n-type or p-type impurities based on the particular end device requirements. In addition, sidewall spacers may optionally be formed prior to the source/drain ion implantation to control the location of the source/drain junctions based on the particular circuit requirements. Activation annealing may then be performed to activate source/drain regions 1010 and 1020.

[0029] The present invention has been described above as forming a tri-gate MOSFET with a number of fin structures. It should be understood that implementations consistent with the present invention may be used to form double or tri-gate devices with other numbers of fins, based on the particular circuit requirements.

[0030] Thus, in accordance with the principles of the invention, a tri-gate MOSFET device may be formed, providing better short-channel control than double and single gate devices. Also, the tri-gate MOSFET may have higher drive current than double-gate devices for the same gate area.

OTHER IMPLEMENTATIONS

[0031] An alternative implementation is directed to improving gate patterning through the use of metal spacers. Figs. 11-14 illustrate exemplary views for forming a FinFET device in an alternative implementation consistent with the principles of the invention. With reference to Fig. 11, the semiconductor device may include a silicon on insulator (SOI) structure with a buried oxide layer 1110 formed on a substrate 1100 and a silicon fin structure 1120 formed on buried oxide layer 1110. Silicon fin structure 1120 may be formed via conventional techniques. For example, a photoresist material may be deposited and patterned to form a photoresist mask. The silicon layer may then be etched in a conventional manner, with the etching terminating on buried oxide layer 1110, to form silicon fin structure 1120.

[0032] A metal layer 1210 may then be deposited on the semiconductor device, as illustrated in Fig. 12. In one implementation, the metal layer 1210 may comprise tungsten, titanium, tantalum, or nickel. Other metals may alternatively be used.

[0033] Metal layer 1210 may then be patterned and etched to form spacers 1310, as illustrated in Fig. 13. As illustrated, spacers 1310 are formed on opposite sides of silicon fin structure 1120. A gate material layer 1410 may then be deposited to form one or more gate electrodes, as illustrated in Fig. 14. In an exemplary implementation, gate material layer 1410 may include polysilicon deposited using conventional CVD. Alternatively, other semiconducting materials, such as germanium or combinations of silicon and germanium, or various metals may be used as the gate material. The gate material layer 1410 may then be

patterned and etched to form gate electrodes. Metal spacers 1310 act to reduce the fin step height during gate patterning, thereby improving gate patterning.

[0034] In another implementation, an alternative filling material may be used in fabricating a damascene gate MOSFET. As illustrated in Fig. 15, a semiconductor device may include an oxide layer 1510 formed on a substrate (not shown) with a silicon layer 1520 formed thereon. A dummy polysilicon gate 1530 may be formed on silicon layer 1520. A spacer material, such as a silicon oxide (e.g., SiO_2), may be deposited and etched to form spacers 1540 on the side surfaces of dummy polysilicon gate 1530. An organic material 1550 may then be deposited and planarized to expose the top surface of dummy polysilicon gate 1530.

[0035] Dummy polysilicon gate 1530 may then be removed. A metal gate 1610 may then be deposited and polished, as illustrated in Fig. 16. The metal may include, for example, tungsten, tantalum nitride, tantalum silicon nitride, titanium, or nickel. Other metals may alternatively be used. Organic material 1550 may then be removed and the source and drain regions may be silicided 1620. In one implementation, silicide 1620 may be NiSi or $CoSi_2$.

CONCLUSION

[0036] Implementations consistent with the principles of the invention provide a tri-gate MOSFET device that provides better short-channel control than double and single gate device designs.

[0037] The foregoing description of exemplary embodiments of the present invention provides illustration and description, but is not intended to be exhaustive or to limit the invention to the precise form disclosed. Modifications and variations are possible in light of the above teachings or may be acquired from practice of the invention. For example, in the above descriptions, numerous specific details are set forth, such as specific materials, structures, chemicals, processes, etc., in order to provide a thorough understanding of the present invention. However, the present invention can be practiced without resorting to the details specifically set

forth herein. In other instances, well known processing structures have not been described in detail, in order not to unnecessarily obscure the thrust of the present invention. In practicing the present invention, conventional deposition, photolithographic and etching techniques may be employed, and hence, the details of such techniques have not been set forth herein in detail.

[0038] While a series of acts has been described with regard to Fig. 1, the order of the acts may be varied in other implementations consistent with the present invention. Moreover, non-dependent acts may be implemented in parallel.

[0039] No element, act, or instruction used in the description of the present application should be construed as critical or essential to the invention unless explicitly described as such. Also, as used herein, the article "a" is intended to include one or more items. Where only one item is intended, the term "one" or similar language is used.

[0040] The scope of the invention is defined by the claims and their equivalents.